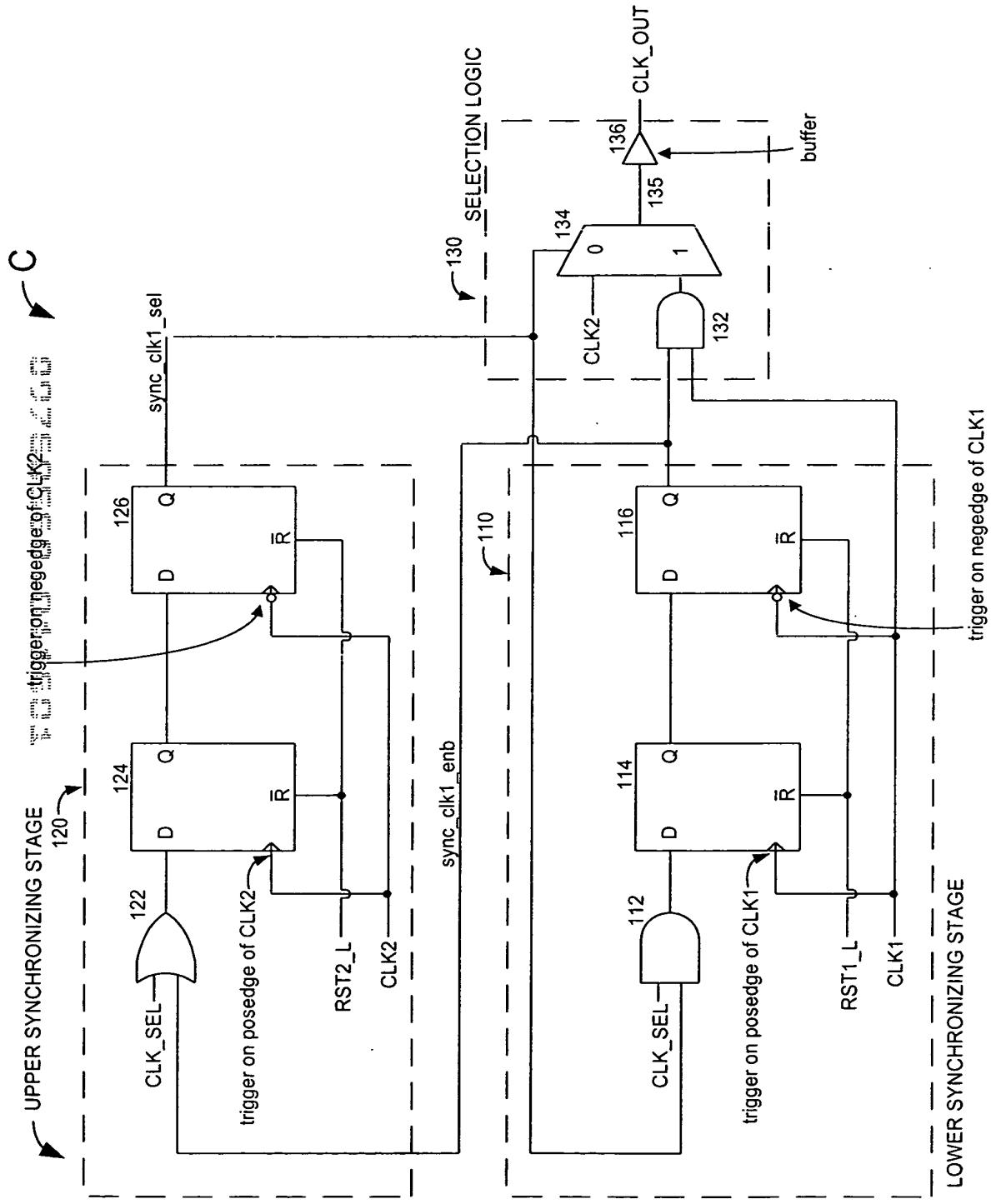


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Figure 2a



Synthesized (gate implementation) schematic from Verilog RTL

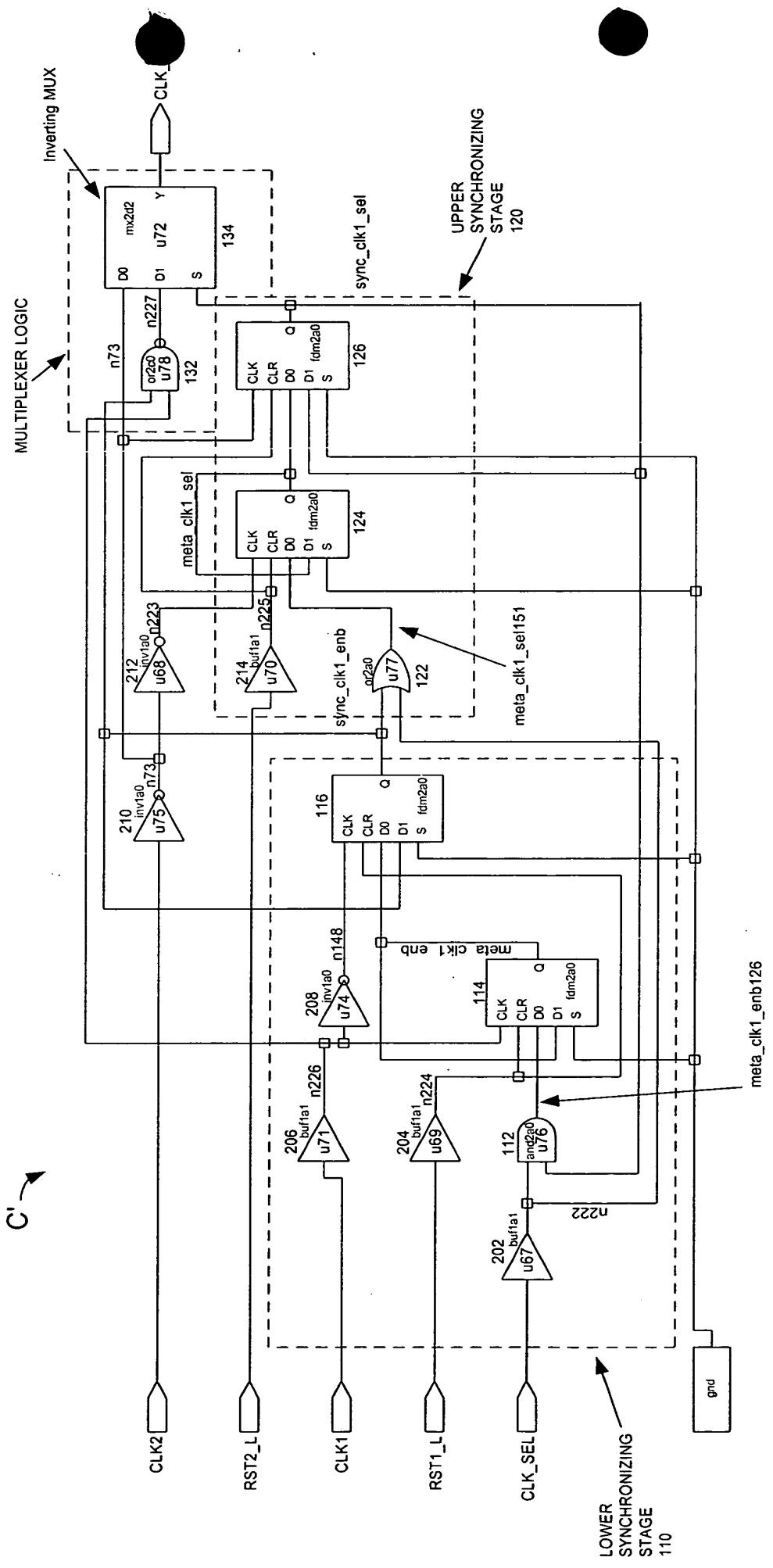
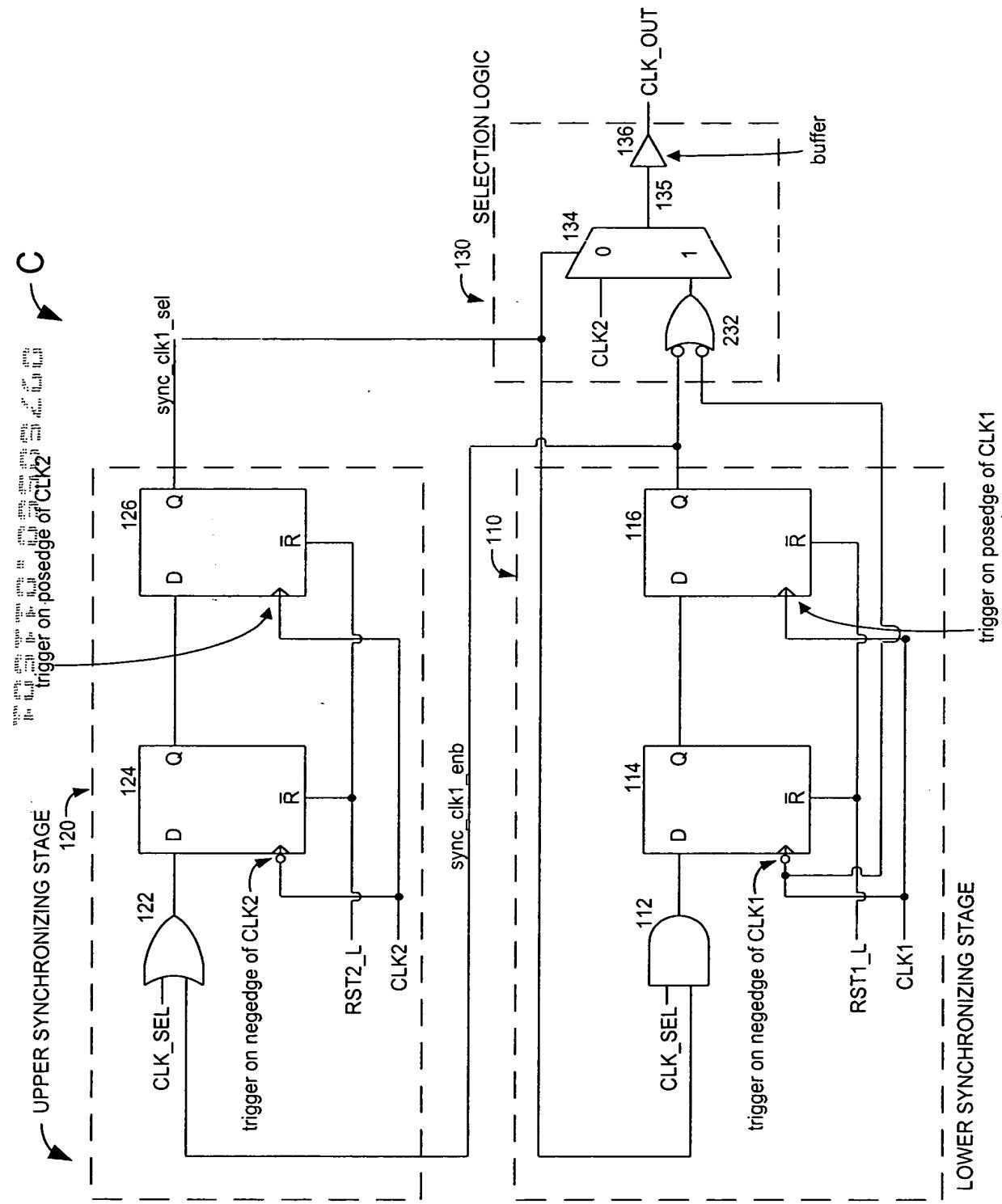


Figure 2b

Figure 2c



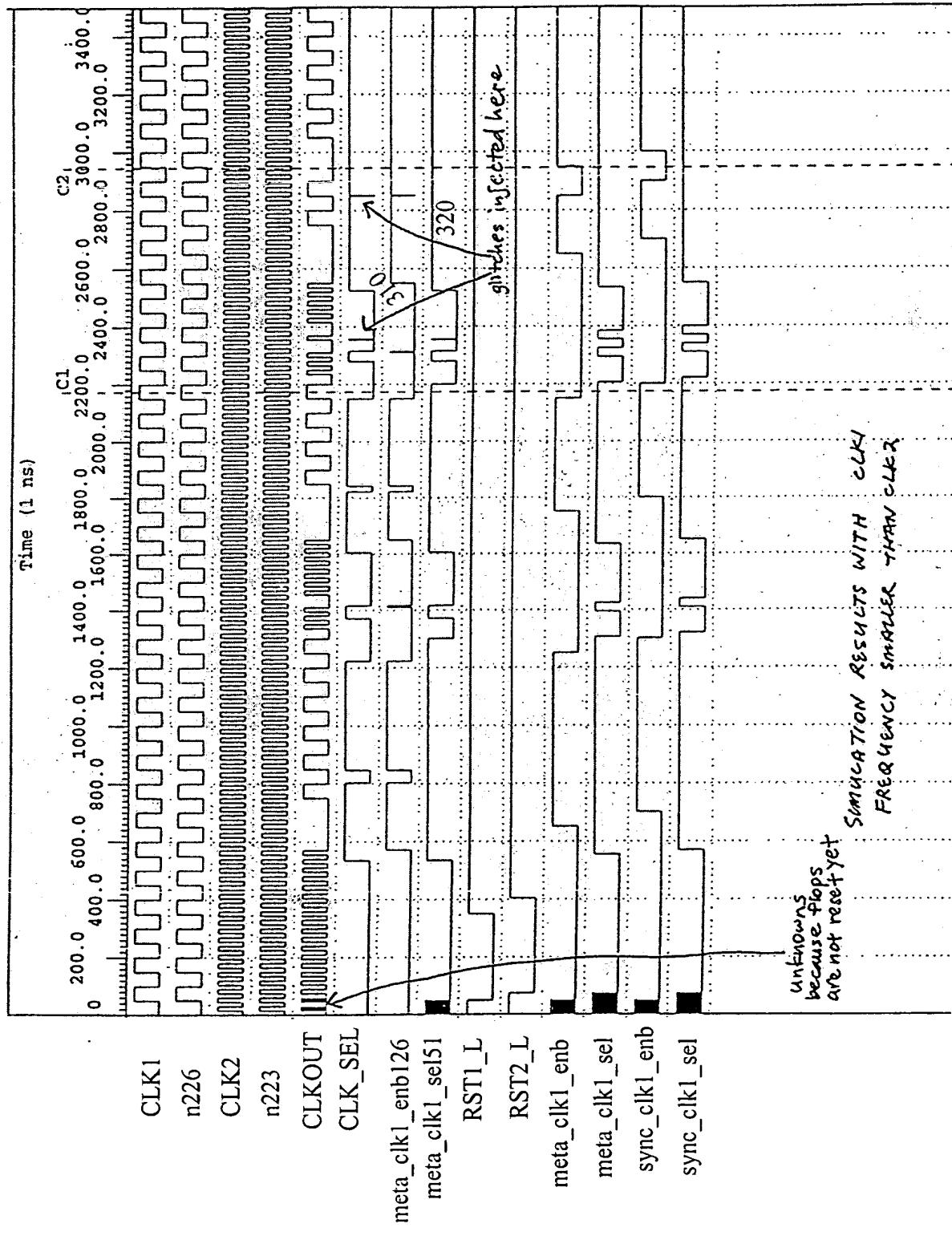


Figure 3

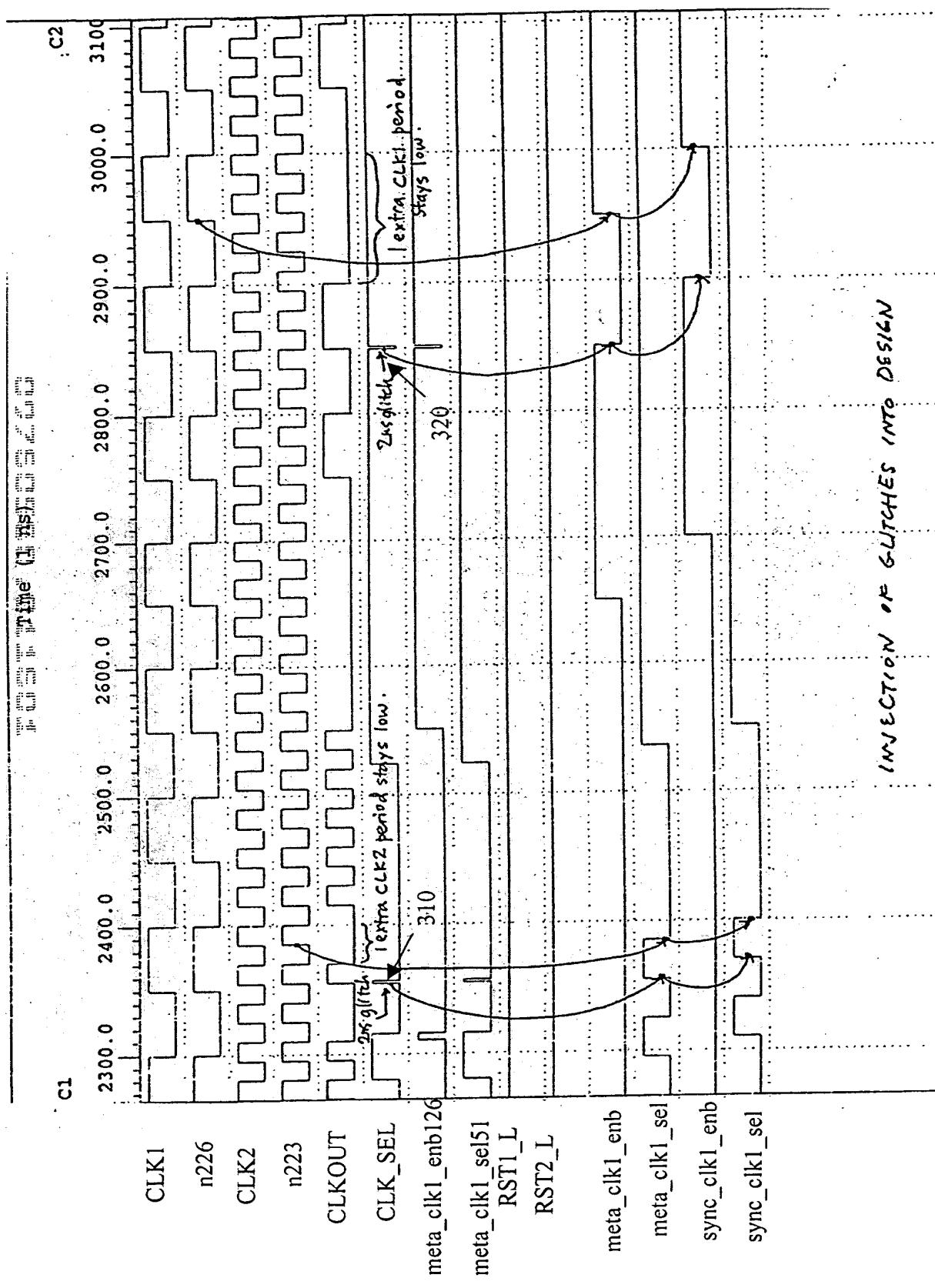


Figure 4

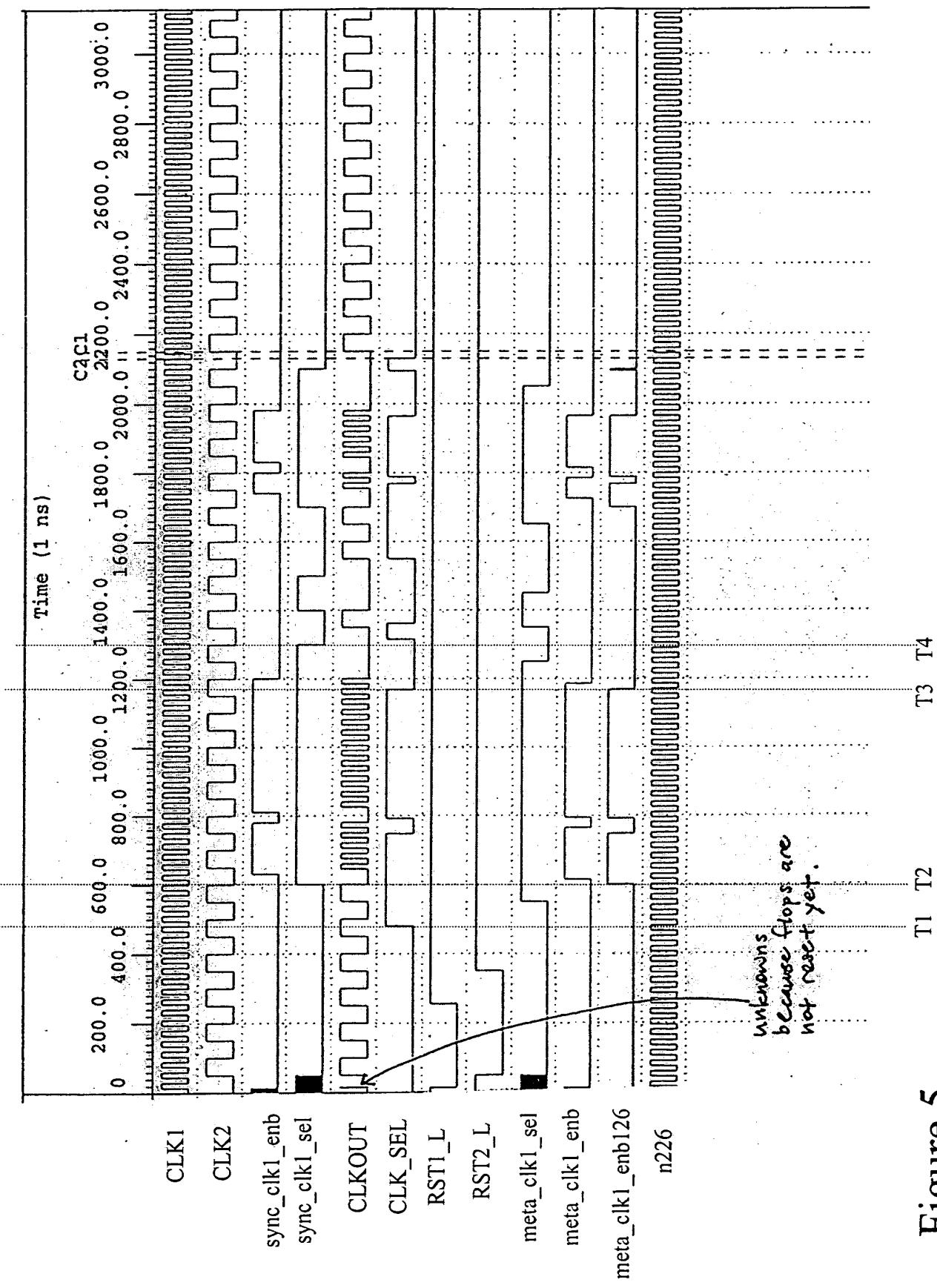


Figure 5